Claims 1 & 2 OK for 710/100 AA A.U. 2191 5/27/2007

WHAT IS CLAIMED IS:

1. A bus structure for connection between a control circuit and plural circuits to be controlled in a semiconductor integrated circuit, comprising:

an address bus divided into an upstream bus and a downstream bus; and

a data bus divided into an upstream bus and a downstream bus.

2. The bus structure of Claim 1,

wherein said data bus is divided with respect to each of said plural circuits to be controlled and each divided portion of said data bus is further divided into an upstream bus and a downstream bus.

3. A database for use in design of a semiconductor integrated circuit comprising:

a table including description of kinds of bus structures for connection between a control function part and plural applications.

4. The database of Claim 3,

wherein said table includes a performance table describing a performance index for evaluating performance attained by an operation model of each of said applications.

5. The database of Claim 4,

wherein said performance table includes, as said performance index, at least one of parameters of throughput, a bus width,

instruction quantity and memory size.

6. The database of Claim 3,

wherein said performance table includes, as the description of kinds of bus structures, description of a separate type bus structure having an address bus divided into an upstream bus and a downstream bus and a data bus divided into an upstream bus and a downstream bus.

7. A method of designing an interface for connection between a control function part of a semiconductor integrated circuit and plural applications by using a database storing plural libraries corresponding to operation models of said plural applications, comprising a step of:

analyzing a number of collisions of bus transaction through operation simulation where said applications are limitlessly operated by said control function part by successively using each of said plural libraries as the operation model of each of said plural applications.

8. The method of designing an interface of Claim 7, further comprising a step of generating FIFOs in a number of stages according to the number of collisions of bus transaction,

wherein the number of collisions of bus transaction is analyzed with the FIFOs virtually inserted between said applications.

9. A method of designing an interface for connection between a control function part of a semiconductor integrated circuit and

plural applications by using a database storing plural libraries corresponding to operation models of said plural applications, comprising a step of:

analyzing a number of concurrent instruction processing through operation simulation where said applications are limitlessly operated by said control function part by successively using each of said plural libraries as the operation model of each of said plural applications.

10. The method of designing an interface of Claim 9,

wherein a structure of a cross bar bus is determined in accordance with the number of concurrent instruction processing.

11. The method of designing an interface of Claim 10, further comprising a step of generating a transfer operation control function part to be disposed in a bus where the number of concurrent instruction processing is larger than a value,

wherein the number of concurrent instruction processing is analyzed with the transfer operation control function part disposed in the bus.

12. A method of designing an interface for connection between a control function part of a semiconductor integrated circuit and plural applications by using a database storing plural libraries corresponding to operation models of said plural applications and plural bus structures, comprising the steps of:

(a) setting plural main parameters for ultimately evaluating said semiconductor integrated circuit and setting plural

sub-parameters affecting each of said main parameters;

(b) selecting library groups where said main parameters meet target values by evaluating each of said main parameters on the basis of said sub-parameters of each of said libraries; and

(c) determining an interface by selecting an optimal library group by evaluating plural main parameters determined with respect to each of said selected library groups.

13. The method of designing an interface of Claim 12, further comprising, before the step (a), a step of analyzing said sub-parameters of each of said libraries through operation simulation conducted by successively using each of said plural libraries as an operation model of each of said plural applications.

14. The method of designing an interface of Claim 12,

wherein, in the step (a), three main parameters are set and three sub-parameters are set with respect to each of said three main parameters;

in the step (b), a three-dimensional coordinate system having said three sub-parameters as coordinate axes is built for selecting a library group where an area of a triangle determined according to values of said sub-parameters is smaller than a target value; and

in the step (c), a three-dimensional coordinate system having said three main parameters as coordinate axes is built for determining said interface based on a library group where an area of a triangle determined according to values of said main parameters

obtained from said selected library groups is minimum.

15. The method of designing an interface of Claim 12, further comprising, after the step (a) and before the step (b), a step of selecting a library group where a specific sub-parameter noticed among said plural sub-parameters meets a target value,

wherein, in the step (b), a library group where main parameters excluding a specific parameter among said plural main parameters meet target values is selected, and

in the step (c), a library group where said specific main parameter is minimum is selected as said optimal library group.

16. The method of designing an interface of Claim 12,

wherein, in the step (a), affecting coefficients of said plural sub-parameters affecting said main parameters are respectively set,

in the step (b), a library group where said main parameters meet target values is selected on the basis of said affecting coefficients and values of said sub-parameters; and

in the step (b), plural main parameters obtained from said selected library groups are weighted before selecting said library group where said main parameters meet the target values.

17. A method of designing an interface for connection between a control function part of a semiconductor integrated circuit and plural applications by using a database storing plural libraries corresponding to operation models of said plural applications and plural bus structures, comprising the steps of:

(a) successively selecting each of said plural libraries as the operation model of each of said plural applications;

(b) operating said plural applications by said control function part, whereby analyzing performances of said control function part, an interface and said applications attained by using each of said libraries;

(c) repeatedly conducting the steps (a) and (b), whereby determining an interface by selecting an optimal library group on the basis of results of the analysis; and

(d) synthesizing an optimal interface on the basis of said determined parameters.

18. The method of designing an interface of Claim 17,

wherein, in the step (b), a number of collisions of bus transaction occurring by limitlessly operating said applications by said control function part is analyzed with respect to each of said libraries, and

in the step (d), FIFOs in a number of stages according to the number of collisions of bus transaction are inserted between said applications.

19. The method of designing an interface of Claim 17,

wherein, in the step (b), a number of concurrent instruction processing occurring by limitlessly operating said applications by said control function part is analyzed with respect to each of said libraries, and

in the step (d), a cross bar bus is disposed in a bus where

the number of concurrent instruction processing is larger than a value.